

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1.-3 (Canceled)

4. (New) A semiconductor device manufacturing method comprising the steps of:

manufacturing wafers in a manufacturing line using predetermined manufacturing processed, each of said wafers having a plurality of semiconductor chips provided therein in a grid-like arrangement;

testing said plurality of semiconductor chips for electric characteristics thereof;

writing into each of said plurality of semiconductor chips, information of a chip position on said wafer associated with said testing;

storing a first test result from said testing step and storing said chip position information that is associated with said first test result;

dividing said wafer into respective ones of said semiconductor chips to produce semiconductor devices each sealed in a package;

testing each of said semiconductor devices for its electric characteristics to produce second test results;

detecting stored position information of each of said semiconductor devices associated with said second test results after said semiconductor device has been sealed in a package;

storing said second test results and said associated information of said semiconductor device position; and

mapping the distribution of failures corresponding to a wafer by combining position information of those chips determined to be faulty in said semiconductor chip testing step and

position information of those semiconductor devices determined to be faulty in said semiconductor devices testing step, based on said first test result, said second test result and said information of chip position and semiconductor device position;

determining a cause of failures based on said distribution of failures.

5. (New)A semiconductor device manufacturing method comprising the steps of:

manufacturing a wafer in a manufacturing line, said wafer having a plurality of semiconductor memories provided therein in a grid-like arrangement;

wafer testing said semiconductor memories for electric characteristics thereof;

determining in a trimming device a redundancy address for a redundancy memory of each semiconductor memory and blowing fuses corresponding to said redundancy address;

storing, in a wafer test information storage device, said redundancy address and position information on said wafer of said redundancy memory that is associated with said redundancy address;

dividing, in a package assembling device, said wafer into respective ones of said semiconductor memories to produce semiconductor memories each sealed in a package;

after said dividing step, testing, in a product tester, each semiconductor memory for its electric characteristics and reading a replacement address;

estimating, in a position estimating device, position information by comparing said read replacement address with said redundancy address;

storing, in a product test information storage device, a second test result outputted from said product tester and said position information detected by said position estimating device that is associated with said second test result;

mapping, in a failure distribution mapping device, the distribution of failures by associating said second test result with said position information; and

determining a cause of failures based on said distribution of failures.

6. (New) A semiconductor device manufacturing method comprising the steps of:

manufacturing, in a manufacturing line, a wafer with a plurality of semiconductor memories provided therein in a grid-like arrangement;

testing, in a wafer tester, said semiconductor memories for electric characteristics thereof;

determining, in a trimming device, a replacement address for a redundancy memory of each semiconductor memory and blowing fuses corresponding to said replacement address;

storing, in a position information storage device, said replacement address and position information on said wafer that is associated with said replacement address;

dividing, in a package assembling device, said wafer into respective ones of said semiconductor memories to produce semiconductor memories each sealed in a package;

testing, in a product tester, each semiconductor memory for its electric characteristics and reading a replacement address;

estimating, in a position estimating device, position information by comparing said read replacement address with said replacement address stored in said position information storage device;

storing, in a product test information storage device, a first test result outputted by said wafer tester, a second test result outputted from said product tester and said position information on said wafer estimated by said position estimating device in association with one another;

mapping, in a failure distribution mapping device and based on said first test result, said second test result and said position information, the distribution of failures by combining position information of those semiconductor memories determined to be faulty by said wafer

tester and position information of those semiconductor memories determined to be faulty by said product tester; and

determining a cause of failures based on said distribution of failures.

7. (New) A semiconductor device manufacturing method for estimating the location of a cause of a failure based on a test result of a manufactured semiconductor device comprising the steps of:

electronically reading, in a position information reading device, chip data previously written in a predetermined circuit of said semiconductor device after this semiconductor device has been sealed into a package;

extracting, in a position information extracting device, a lot number of said semiconductor device in a wafer process, a wafer number of a wafer in said lot and position information on said wafer based on said chip data; and

determining, in a failure cause determining device, a cause of a failure which has occurred after division of said wafer into chips by combining respective test results before and after said division into a single distribution of failures.

8. (New) A semiconductor device manufacturing system according to claim 7, wherein said determining step determines a cause of a failure in a wafer process based on said position information of that semiconductor device which is determined to be faulty in a test of semiconductor devices after sealing into packages.

9. (New) A semiconductor device manufacturing system according to claim 7, wherein said position information is a replacement address for replacing a faulty memory cell, said method further comprising the steps of:

generating, in a reference table mapping device, a reference table showing a relation between said position information and said replacement address in a test for determining whether a semiconductor device in a wafer state is faulty or non-defective, and

extracting, in said position information extracting device, position information of said semiconductor device after sealing into a package from said reference table based on address data read from said sealed semiconductor device.

10. (New) A semiconductor device manufacturing method according to claim 7, further comprising the steps of:

storing, using a data writing device, trimming data in a storage circuit during a test for determining whether a semiconductor device in a wafer state is faulty or non-defective;

reading, in a data reading device, said trimming data from said storage circuit;

mapping, in a reference table mapping device, a reference table showing a relation between said position information and said trimming data; and

extracting, using said position information extracting device and based on trimming data read from said semiconductor device, said position information of semiconductor devices corresponding to the trimming data from said reference table.